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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,519	09/24/2001	Koutarou Tagawa	1448.1015	7245

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EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,519	TAGAWA ET AL.	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,10,11 and 15* is/are rejected.

7)☒ Claim(s) *2-4,7-9 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/24/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Office Action

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 6, and 10, are rejected under 35 U.S.C. 102(e) as being anticipated by Nagatome, U.S. Patent 6,339,753 B1.

Referring to claim 1:

a. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU and an in-circuit emulator (a microcomputer with a debug supporting function in which a program to be executed by a CPU is debug using an in-circuit emulator).

b. In column 3, lines 62-66, Nagatome discloses that the simulator chip includes a CPU block and a peripheral block. A first power supply is connected to the designation unit and the CPU block, while a second power supply is connected to the peripheral block and the microcomputer application system (a debug target circuit which has the CPU and in which supply and stop of drive power can be arbitrarily switched).

c. In column 3, lines 57-61, Nagatome discloses that the in-circuit emulator includes a simulator chip that simulates the operation of the microcomputer. The in-circuit emulator further includes a designation unit, which is realized with a RAM or the like, simulating a read only memory (ROM) in the microcomputer application system. The designation unit is designed to supply instruction signals to the simulator chip (a debugging circuit which has an interface module to the in-circuit emulator and which holds a debug related setting by drive power).

Further, in column 3, lines 62-66, Nagatome discloses a first power supply is connected to the designation unit and the CPU block (holds a debug related setting by drive power supplied in a condition in which power supply to the debug target circuit is stopped).

Referring to claims 5 and 10 in column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU (wherein the microcomputer is a microcontroller or a microprocessor).

Referring to claim 6:

a. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU and an in-circuit emulator (a microcomputer with a debug supporting function in which a program to be executed by a CPU is debug using an in-circuit emulator).

b. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU (a debug target circuit which has the CPU).

c. In column 3, lines 57-61, Nagatome discloses that the in-circuit emulator includes a simulator chip that simulates the operation of the microcomputer. The in-circuit emulator further includes a designation unit, which is realized with a RAM or the like, simulating a read only memory (ROM) in the microcomputer application system. The designation unit is designed to supply instruction signals to the simulator chip (a debugging circuit which has an interface module to the in-circuit emulator).

d. In column 3, lines 62-66, Nagatome discloses that a second power supply is connected to the peripheral block and the microcomputer application system (a first power supply terminal which supplies an external drive power to the debug target circuit).

e. In column 3, lines 62-66, Nagatome discloses that the simulator chip includes a CPU block and a peripheral block. A first power supply is connected to the designation unit and the CPU block (a second power supply terminal which supplies an external drive power to the debugging circuit independent of power supply to the debug target circuit).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagatome U.S. Patent 6,339,753 B1.

Referring to claim 11:

a. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU and an in-circuit emulator (a microcomputer with a debug supporting function in which a program to be executed by a CPU is debug using an in-circuit emulator).

b. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU (a debug target circuit which has the CPU).

c. In column 3, lines 57-61, Nagatome discloses that the in-circuit emulator includes a simulator chip that simulates the operation of the microcomputer. The in-circuit emulator further includes a designation unit, which is realized with a RAM or the like, simulating a read only memory (ROM) in the microcomputer application system. The designation unit is designed to supply instruction signals to the simulator chip (a debugging circuit which has an interface module to the in-circuit emulator).

d. In column 3, lines 62-66, Nagatome discloses that a second power supply is connected to the peripheral block and the microcomputer application system (a first power supply terminal which supplies an external drive power to the debug target circuit).

e. In column 3, lines 62-66, Nagatome discloses a power supply. However, Nagatome doesn't explicitly disclose a switching element which switches supply

and stop of the external drive power supplied through the power supply terminal to the debug target circuit; and a switch control terminal to which a control signal for controlling the switching of the switching element is supplied from outside.

The Examiner takes Official Notice that it a switch for controlling the power supply of a CPU is well known. An example of this is the power switch/button located on the outside of the case for the computer. It would have been obvious to one of ordinary skill at the time of the invention to include a power switch into the system of Nagatome. A person of ordinary skill in the art would have been motivated to make the modification because a switch gives the user the ability to switch the power on and off without having to unplug the power supply from an electrical outlet or battery. The design is simplified and more convenient to a user.

Referring to claim 15 in column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU (wherein the microcomputer is a microcontroller or a microprocessor).

Allowable Subject Matter

5. Claims 2, 3, 4, 7, 8, 9, 12, 13, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP 02002358212A	Tagawa et al.
US 2003/0074180 A1	Shibayama et al.
US 2002/0147939 A1	Wenzel et al.
U.S. Patent 6,044,476	Ote et al.
U.S. Patent 5,935,266	Thurnhofer et al.
U.S. Patent 5,283,905	Saadeh et al.
U.S. Patent 5,226,047	Catlin

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

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